SHALLOW TRENCH ISOLATION STRUCTURE WITH LOW TRENCH PARASITIC CAPACITANCE

ABSTRACT OF THE DISCLOSURE

Provided are methods and composition for forming an isolation structure on an integrated circuit substrate. First, a trench is etched in the integrated circuit substrate. A lower dielectric layer is then formed in the trench such that the lower dielectric layer at least partially fills the trench. An upper dielectric layer is then formed over the lower dielectric layer to create an isolation structure, the upper dielectric layer and the lower dielectric layer together having an effective dielectric constant that is less than that of silicon dioxide, thereby enabling capacitance associated with the isolation structure to be reduced.